PERSONAL INFORMATION

Georgios Lentaris

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http:

Sex Male | Nationality Greek

WORK EXPERIENCE

January 2023 – present

Assistant Professor

University of West Attica, dpt. of Informatics & Computer Engineering (www.ice.uniwa.gr), Athens, GR.

- Field: design of hardware units for digital signal processing systems
- Research and Teaching

February 2013 – present

Sr. Research Associate

National Technical University of Athens, school of ECE, microprocessors lab (www.microlab.ntua.gr), and Institute of Communication & Computer Systems (ICCS/ECE/NTUA), Zografou, Athens, Greece.

- HW/SW co-design and high-performance embedded computing on FPGA and DSP processors
- space/avionics applications, edge computing, telecom (system design on single-/multi-/SoC-devices)
- DSP acceleration and VHDL circuit development (for computer vision, image/video, telecom, AI, etc.)
- reliability of FPGA devices (including radiation testing)
- proposal writing and technical coordination of projects
- teaching associate

May 2012 – February 2013

Military Service

Hellenic Army Supreme Military Support Command - DYB, Athens, Greece.
Research and Informatics Corps

- computer network development and support
- IT specialist

September 2011 – May 2012

Research Assistant

National Technical University of Athens, school of ECE, microprocessors lab (www.microlab.ntua.gr), with assist. prof. Dimitrios Soudris, Zografou, Athens, Greece.

- HW/SW co-design of computer vision for space rover navigation (for the European Space Agency)

September 2004 – August 2011

Research/PhD

National & Kapodistrian University of Athens, Physics Dpt, Electronics lab (dst.phys.uoa.gr), with assist. prof. Dionysios Reisis, Zografou, Athens, Greece.

- parallel architectures, digital circuit design, FPGA implementations, DSP algorithms

EDUCATION AND TRAINING

2006 – 2011

PhD in Computing
Thesis title: “Parallel Architectures and Algorithms for Digital Signal and Image Processing”

National & Kapodistrian University of Athens, Physics Dpt, Electronics lab
Advisors: assistant prof. D. Reisis, prof. A. Katsaggelos, prof. G. Tombras

- The research involved digital circuit design, digital signal processing, FPGA platforms, parallelization techniques, with studies both on theoretical and practical level. The thesis focused on designing parallel memories for image processing and motion estimation architectures for video compression

2006 – 2010

MSc in “Logic, Algorithms, and Computation”

National & Kapodistrian University of Athens, Departments of Mathematics & Informatics, Greece
National Technical University of Athens, Schools of ECE & SEMFE, Greece

- 2-year graduate programme in the field of Theoretical Computer Science. The courses covered many aspects of algorithmic design, complexity analysis, discrete mathematics, informatics, etc. Major in "Computer Science Logic" (http://mpla.math.uoa.gr/en/)

2004 – 2006

MSc in “Electronic Automation”

National & Kapodistrian University of Athens, Departments of Physics & Informatics, Greece

- 2-year graduate programme in the general field of Computer Science/Engineering. The courses covered many aspects of computer programming, digital design, networks, systems, informatics, etc.

1999 – 2004

BSc in Physics

National & Kapodistrian University of Athens, Department of Physics, Greece

- 4-year programme. Major in "Electronics, Computers, Telecommunications, and Automation"

PERSONAL SKILLS

Mother tongue(s): Greek

Other language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
English	C1	C1	C1	C1	C1
	Cambridge English First Certificate (FCE/lower) and numerous papers/lectures in English journals/conferences				
French	A1	A1	A1	A1	A1
	basic training in high-school classes				

Levels: A1/A2: Basic user - B1/B2: Independent user - C1/C2 Proficient user
Common European Framework of Reference for Languages

Communication skills

- Team work: strong background in collaboration within small teams of developers (3-6 persons) through numerous projects, experience on collaboration between teams for big European projects
- Teaching: classes of 10-100 students for 10+ years (including preparation of material)
- Mentoring: guidance/assistance of >10 students at various levels (undergraduate, postgrad, PhD)
- Extroversion/Networking: participation in multiple events abroad (conferences, workshops, cluster meetings, project meetings, e-classes) and preparation of future partnerships (projects, experiments)

Organisational / managerial skills

- Leadership: responsible for small teams of developers/researchers (3-6 people, ESA and EC projects), mentoring of PhD students at NTUA, co-planning of future steps for the lab (NTUA)
- Management: assist the administration of all ESA activities of *microlab* (NTUA), technical coordinator of ESA & H2020 projects (e.g., HIPNOS, AI@EDGE), preparation of proposals related to FPGA, space applications, etc., logistics/planning for team members

Job-related skills

- 11 years of experience as a senior researcher at NTUA (post-doc), including technical work & coding, research/experimental activities, project coordination, student mentoring, proposal writing
- teaching associate and assistant in multiple university courses (see section “teaching experience”)
- 60+ publications in peer-reviewed journals and conferences (see section “publications”)
- 13+ presentations in international conferences and workshops (see section “talks/presentations”)
- 11+ years of experience in space-related activities and projects funded by the European Space Agency (13 ESA projects, including mission preparation/study, participation in ESA workshops, and systematic interaction with space-industry in Greece and abroad), as well as EU H2020 projects
- 5 distinct radiation tests/experiments at various facilities across Europe, involving multi-part

collaboration and interdisciplinary skills
- CERN 2017: heavy-ion irradiation of Zynq7000 at SPS (1st external use for such energies)
- Napoli IT 2018: beta-particle irradiation of Zynq7000 at INFN
- ESTEC NL 2018: gamma-ray irradiation of Zynq7000 at ESA Co-60 facility
- ESTEC NL 2022: gamma-ray irradiation of Coral TPU at ESA Co-60 facility
- PSI CH 2022: proton irradiation of Coral TPU at PIF (1st such public results for TPU, TBC)

Digital skills

SELF-ASSESSMENT				
Information processing	Communication	Content creation	Safety	Problem solving
Proficient	Proficient	Proficient	Proficient	Proficient

Levels: Basic user - Independent user - Proficient user
Digital competences - Self-assessment grid

- programming languages: ANSI C, C++, VHDL, MPI, Java, Pascal, Fortran, Basic, Prolog, Assembly, SQL, MATLAB, Simulink, Mathematica, shell scripts, HTML
- operating systems: LINUX/UNIX , Windows/MS-DOS
- digital system development: on FPGA using schematic editors, hardware description languages, and high-level synthesis tools (Xilinx, Altera, Mentor Graphics, Synopsys)
- good command of office suite (word processor, spread sheet, presentation software), typesetting document systems (latex), and photo editing software

Other skills: Music (keyboards), Sports (football, tennis, etc.)

Driving licence: B

ADDITIONAL INFORMATION

Funded Projects (work experience)

18 "*SS4TB, 4S System Services Test Bed (Phase 1)*", ref. ARTES 3A.149/4S.010, European Space Agency (develop PHY layer and interfaces for a 5G testbed using SDR, 2022-2024)

17 "*CAIRS21, COTS AI accelerators in mixed-criticality high-performance avionics for reconfigurable satellites*", ref. 4000135491/21/NL/GLC/ov, European Space Agency (evaluate/design AI for avionics with novel embedded devices such as Google TPU, 2022)

16 "*AI@EDGE, A Secure and Reusable Artificial Intelligence Platform for Edge Computing in Beyond 5G Networks*", European Commission, H2020-ICT-52, GA 101015922 (acceleration of AI/ML functions on FPGA and GPU platforms over virtualization & serverless, 2021-2023)

15 "*QUEENS2*" and "*QUEENS3*", ref. RFP/3-16086/19/NL/RA/va & 4000134874/21/NL/AR/va, European Space Agency (tool assessment, benchmarking, development on the new Nanoxplore/NG/BRAVE LARGE FPGA and ULTRA FPGAs, 2019-2023)

14 "Improved Performance of Reconfigurable Proc. System via Methodology Exploiting Process Variability", MIS 5049182, ΕΔΒΜ 103, Young Researchers' Support (ESF/ESPA, 2020-2022)

13 "*NXARTAN*" and "*LEOTOME*", ref. 4000126305/NL/RA/ig and ref. 4000126083/18/NL/FE, European Space Agency (port previously developed CV algorithms to new embedded comp. devices, i.e., the European NG-LARGE FPGA and the Myriad2 VLIW processor, 2019)

12 "*5G integrated Fiber-Wireless networks exploiting existing photonic technologies for high-density SDN-programmable network architectures*", European Commission, H2020-ICT-2016-2, ICT-08-2017 5G PPP Convergent Technologies, GA 761989 (5GPHOS, integrated Fiber-Wireless networks with DSP implementation on FPGA, 2017-2020)

11 "*Quality Evaluation of European New SW for BRAVE*", ESTEC ref. 4000119331/17/NL/PS, European Space Agency (QUEENS-FPGA, benchmarking and development on the new Nanoxplore/NG/BRAVE FPGA, 2017-2018)

10 "*High Performance Avionics Solution for Advanced and Complex GNC Systems*", ESTEC ref. 4000117700/16/NL/LF, European Space Agency (HIPNOS, avionics architecture design and development of computer vision tasks on SoC-FPGA for space applications, 2016-2017)

9 "*Code Optimisation and Modification for Partitioning of Algorithms developed in SPARTAN/SEXTANT*", ESTEC ref. 4000111213/14/NL/PA , European Space Agency (COMPASS, optimization and multi-FPGA partitioning of computer vision tasks, 2014-2016)

8 "*Spartan EXTension Activity*", ESTEC ref. 4000103357/11/NL/EK, European Space Agency (SEXTANT, real-time HW/SW design of computer vision algorithms on FPGA, 2012-2013)

7 "*Sparing Robotics technologies for Autonomous Navigation*", ESA/ESTEC ITT reference AO/1-6512/10/NL/EK, European Space Agency (SPARTAN, HW/SW co-design of computer vision algorithms for rovers on Mars, 2011-2013)

6 "*Demozed1*", ESTEC purchase order no. 5001022480, European Space Agency (reliability evaluation of the Zynq FPGA and radiation testing of COTS FPGAs, 2018)

5 *"Next Generation Millimeter Wave Backhaul Radio",* MICRO2-ΣΕ-Β/Ε-ΙΙ, Hellenic Funds & ERDF, Hellenic Technology Clusters in Microelectronics - Phase-2 Aid Measure, HSIA "Corallia" (Nexgen-Miliwave, design of a wireless transceiver on FPGA, 2010)

4 Network of Excellence in Wireless Communications++ (NEWCOM++, research for reconfigurable wireless communications, 2009)

3 "*Advanced real-time video encoder*", General Secretariat for Research and Technology, 05ΠΑΒ181, PAVET (VLSI/FPGA optimization of a real-time h264 video encoder, 2006)

2 "*Integration of an H.264 encoder in the platform of INOS*", Information Societies Technology, IST-2002-507794-INOS (INOS, design of a VLSI H.264/AVC encoder, 2004)

1 "*High performance digital processing and electronics for audio and Home Theatre applications*", Information Societies Technology, IST-1999-20380 (HIPRO, audio DSP, 2002)

Publications (scientific Journals)

21 *"End-to-End Real-Time Service Provisioning Over a SDN-Controllable Analog mmWave Fiber-Wireless 5G X-Haul Network",* Vagionas, Maximidis, Stratakos, Margaris, Mesodiakaki, Gatzianas, Kanta, Toumasis, Giannoulis, Apostolopoulos, Papatheofanous, Lentaris, Reisis, Soudris, et el., IEEE Journal of Lightwave Technology, vol.41, no.4, pp.1104-1113, 2023

20 *"Design Space Exploration on High-Order QAM Demodulation Circuits: Algorithms, Arithmetic and Approximation Techniques", I. Stratakos, V. Leon, G. Armeniakos, G., Lentaris, and D. Soudris, MDPI, Electronics, 11(1), p.39., 2022*

19 *"Development and Testing on the European Space-Grade BRAVE FPGAs: Evaluation of NG-Large Using High-Performance DSP Benchmarks",* V. Leon, I. Stamoulias, G. Lentaris, D. Soudris, D. Gonzalez-Arjona, R. Domingo, D.M. Codinachs, and I. Conway, IEEE Access, 9, pp.131877-131892, 2021

18 *"Process Variability Analysis in Interconnect, Logic and Arithmetic Blocks of 16nm FinFET FPGAs",* E. Taka, K. Maragos, G. Lentaris, D. Soudris, ACM Transactions on Reconfigurable Technology & Systems (TRETS), to appear in vol.14, no.2, pp. 1-30, June 2021

17 "*Improving Performance-Power-Programmability in Space Avionics with Edge Devices: VBN on Myriad2 SoC* ", V. Leon, G. Lentaris, E. Petrongonas, D. Soudris, G. Furano, A. Tavoularis, D. Moloney, ACM Trans. on Embedded Comp. Syst. (TECS), vol.20, no.3, pp.1-23, Apr. 2021

16 *"Analog Fiber-Wireless transmission of IFoF/mmWave over in field deployed legacy PON infrastructure for 5G fronthauling"*, Kanta, Pagano, Ruggeri, Agus, Stratakos, Merchinelli, Vagionas, Toumasis, Kalfas, Giannoulis, Miliou, Lentaris, Apostolopoulos, Pleros, Soudris, Avramopoulos, IEEE/OSA Journal of Optical Communications and Networking, , vol. 12, no. 10, pp. D57-D65 , October 2020

15 "*High-Performance Vision-Based Navigation on SoC FPGA for Spacecraft Proximity Operations*", G. Lentaris, I. Stratakos, I. Stamoulias, D. Soudris, M. Lourakis, X. Zabulis. IEEE Trans. on Circuits and Syst. for Video Tech., vol. 30, no. 4, pp. 1188-1202, April 2020

14 "*Single- and multi-FPGA Acceleration of Dense Stereo Vision for Planetary Rovers*", G. Lentaris, K. Maragos, D. Soudris, M. Lourakis, X. Zabulis. ACM Transactions on Embedded Computing Systems (TECS), vol.18, issue 2, article no. 16, Apr. 2019

13 "*In-the-Field Mitigation of Process Variability for Improved FPGA Performance*", K. Maragos, G. Lentaris, D. Soudris. IEEE Trans. on Computers, vol. 68, no. 7, pp. 1049-1063, July 2019

12 "*TID Evaluation System with on-Chip Electron Source and Programmable Sensing Mechanisms on FPGA*", G. Lentaris, K. Maragos, D. Soudris, F. Di Capua, L. Campajola, M. Campajola, A. Costantino, G. Furano, A. Tavoularis, L. Santos. IEEE Transactions on Nuclear Science, vol. 66, no. 1, pp. 312-319, Jan. 2019

11 *"High performance embedded computing in space: Evaluation of platforms for vision-based navigation"*, G. Lentaris, K. Maragos, I. Stratakos, L. Papadopoulos, O. Papanikolaou, D. Soudris, M. Lourakis, X. Zabulis, D. Gonzalez-Arjona, G. Furano. Journal of Aerospace Information Systems, American Institute of Aeronautics and Astronautics (AIAA), vol. 15, no. 4, pp. 178-192., Feb. 2018

10 *"A flexible, high-performance FPGA implementation of a feed-forward equalizer for optical interconnects up to 112 Gb/s"*, K. Maragos, C. Spatharakis, G. Lentaris, P. Kontzilas, S. Dris,

P. Bakopoulos, H. Avramopoulos, D. Soudris. Journal of Signal Processing Systems, Springer, vol. 88, no. 2, pp. 107-125 , November 2016

9 *"Acceleration Techniques and Evaluation on Multicore CPU, GPU and FPGA for Image Processing and Super-Resolution"*, G. Georgis, G. Lentaris, D. Reisis, Journal of Real-Time Image Processing, Springer, num. 16, pp. 1207–1234 (issue 2019), published July 2016

8 *"HW/SW co-design and FPGA acceleration of visual odometry algorithms for rover navigation on Mars"*, G. Lentaris, I. Stamoulias, D. Soudris, M. Lourakis, IEEE Transactions on Circuits and Systems for Video Technology, vol. 26, no 8, pp.1563-1577, Aug 2016

7 *"Reduced Complexity Super-Resolution for Low-Bitrate Video Compression"*, G. Georgis, G. Lentaris, D. Reisis, IEEE Transactions on Circuits and Systems for Video Technology, vol.26, no.2, pp.332-345, February 2016

6 *"SPARTAN: Developing a Vision System for Future Autonomous Space Exploration Robots"*, Kostavelis, Nalpantides, Boukas, Aviles, Stamoulias, Lentaris, Diamantopoulos, Siozios, Soudris, Gasteratos. Journal of Field Robotics, Willey, vol.31, no.1, pp. 107-140, Oct. 2013

5 *"Design and Comparison of FFT VLSI Architectures for SoC Telecom Applications with Different Flexibility, Speed and Complexity Trade-Offs"*, S. Saponara, M. Rovini, L. Fanucci, A. Karachalios, G. Lentaris and D. Reisis. Circuits Systems and Signal Processing, Springer-Birkhauser Boston, vol. 31, no 2, pp. 627-649, 2012

4 *"A Control-Theoretic Approach for Efficient Design of Filters in DAC and Digital Audio Amplifiers"*, K. Tsakalis, N. Vlassopoulos, G. Lentaris, D. Reisis. Circuits Systems and Signal Processing, Springer-Birkhauser Boston, vol. 30, no. 2, pp. 421-438, April 2011

3 *"A Graphics Parallel Memory Organization Exploiting Request Correlations"*, G. Lentaris, D. Reisis, IEEE Transactions on Computers, Volume 59, Issue 6, pp. 762-775, June 2010.

2 *"A real-time motion estimation FPGA architecture"*, K. Babionitakis, G. Doumenis, G. Georgakarakos, G. Lentaris, K. Nakos, D. Reisis, J. Sifnaios, N. Vlassopoulos, Journal of real-time image processing, Special Issue on Field Programmable Technology, Springer-Verlag, Vol.3, no. 1-2, pp. 3-20, January 2008

J1 "*A real-time H.264/AVC VLSI encoder architecture*", K. Babionitakis, G. Doumenis, G. Georgakarakos, G. Lentaris, K. Nakos, D. Reisis, J. Sifnaios, N. Vlassopoulos, Journal of real-time image processing, Springer-Verlag, Vol.3, no. 1-2, pp. 43-59, November 2007

Publications
(Conference proc., book chapters)

37 "*Combining Fault Tolerance Techniques and COTS SoC Accelerators for Payload Processing in Space*", V. Leon, E.A. Papatheofanous, G. Lentaris, C. Bezaitis, N. Mastorakis, G. Bampilis, D. Reisis, D. Soudris, in Int'l Conf. on Very Large Scale Integration (IFIP/IEEE VLSI-SoC), pp.1-4, Oct. 2022, Patras, Greece. BEST PAPER AWARD

36 "*Towards Employing FPGA and ASIP Acceleration to Enable Onboard AI/ML in Space Applications*", V. Leon, G. Lentaris, D. Soudris, S. Vellas, M. Bernou, in Int'l Conf. on Very Large Scale Integration (IFIP/IEEE VLSI-SoC), pp.1-4, Oct. 2022, Patras, Greece

35 "*Improving the performance of RISC-V softcores on FPGA by exploiting PVT variability and DVFS*", E. Taka, G. Lentaris, D. Soudris, Circuits and Systems, IEEE I'ntl Symp. on (ISCAS), pp 1-4, Texas USA, May 2022

34 *"LSTM Acceleration with FPGA and GPU Devices for Edge Computing Applications in B5G MEC*", Danopoulos D, Stamoulias I, Lentaris G, Masouros D, Kanaropoulos I, Kakolyris AK, Soudris D., Int'l Conference on Embedded Computer Systems 2022, pp. 406-419, Springer, Cham.

33 "*End-to-End Real-Time Service Provisioning over a SDN-controllable 60 GHz analog FiWi X-haul for 5G Hot-Spot Networks*," in Optical Fiber Communication Conference (OFC) 2022, C. Vagionas, R. Maximidis, I. Stratakos, A. Margaris, A. Mesodiakaki, M. Gatzianas, K. Kanta, P. Toumasis, G. Giannoulis, D. Apostolopoulos, E. A. Papatheofanous, G. Lentaris, D. Reisis, D. Soudris, K. Tsagkaris, N. Argyris, D. Syrivelis, P. Bakopoulos, R. M. Oldenbeuving, C. G. H. Roeloffzen, P. W. L. van Dijk, I. Dimogiannis, A. Kontogiannis, H. Avramopoulos, A. Miliou, N. Pleros, G. Kalfas, Technical Digest Series (Optica Publishing Group, 2022), paper Th4A.7

32 "*FPGA & VPU Co-Processing in Space Applications: Development and Testing with DSP/AI Benchmarks*", V. Leon, C. Bezaitis, G. Lentaris, D. Soudris, D., Reisis, E.A. Papatheofanous, A. Kyriakos, A., Dunne, A., Samuelsson, and D. Steenari, in 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pp. 1-5, UAE, Dec. 2021

31 "*Towards sharing one FPGA SoC for both low-levelPHY and high-level AI/ML computing at the edge"*, I. Stratakos, E. A. Papatheofanous, D. Danopoulos, G. Lentaris, D. Reisis, D. Soudris, IEEE Int'l Mediterranean Conf. on Communications and Networking, Workshop on Intelligent operations security and acceleration for edge computing, pp. 76-81, July 2021

30 *"ParalOS: A Scheduling & Memory ManagementFramework for Heterogeneous VPUs",* E.

Petrongonas, V. Leon, G. Lentaris, D. Soudris, 24th Euromicro Conference on Digital System Design (DSD), IEEE proc., pp. 221-228, Sept. 2021

29 "*ApproxQAM: High-Order QAM Demodulation Circuits with Approximate Arithmetic*", V. Leon, I. Stratakos, G. Armeniakos, G. Lentaris, D. Soudris, Modern Circuits and Systems Technologies (MOCAST), IEEE Int'l conf. on, pp.1-4, July 2021

28 "*A PVT-Aware Voltage Scaling Method for Energy Efficient FPGAs",* K. Maragos, G. Lentaris, D. Soudris, Circuits and Systems, IEEE I'ntl Symp. on (ISCAS), pp 1-4, Korea, May 2021

27 "*Combining Arithmetic Approximation Techniques for Improved CNN Circuit Design*", G. Lentaris, G. Chatzitsompanis, V. Leon, K. Pekmestzi, D. Soudris. Electronics, Circuits and Systems, IEEE Int'l Conf. on (ICECS), Scotland, November 2020.

26 "*Fast Packet Classification using RISC-V and HyperSplit Acceleration on FPGA*", A. Pnevmatikou, G. Lentaris, N. Kokkalis, D. Soudris, IEEE Int'l Symp. ISCAS, October 2020

25 *"Analysis of Performance Variation in 16nm FinFet FPGA Devices"*, K. Maragos, E. Taka, G. Lentaris, I. Stratakos, D. Soudris, Field-Programmable Logic and Applications, IEEE Int'l conf. on, FPL 2019, Barcelona Spain, September 2019

24 *"PVT-Aware Sensing and Voltage Scaling for Energy Efficient FPGAs"*, K. Maragos, G. Lentaris, D. Soudris, V. F. Pavlidis, ACM/SIGDA Int'l Symp. on Field-Programmable Gate Arrays (FPGA), poster session, California USA, February 2019

23 "*Parallel Robust Absolute Orientation on FPGA for Vision and Robotics*", N. Dimou, M. Lourakis, G. Lentaris, D. Soudris, D. Reisis. IEEE Int'l Conf. on Electronics, Circuits and Systems (ICECS), pp. 1-4, France, December 2018

22 "*FPGA SEE Test with Ultra-High Energy Heavy Ions*", Furano, Tavoularis, Santos, Ferlet-Cavrois, Boatella, Garcia Alia, Fernandez Martinez, Kastriotou, Wyrwoll, Danzeca, Tali, Gacnik, Kramberger, Juul, Maragos, Lentaris, IEEE Int'l Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 1-4, Chicago USA, October 2018

21 "*Evaluation Methodology and Reconfiguration Tests on the New European NG-MEDIUM FPGA*", K. Maragos, V. Leon, G. Lentaris, D. Soudris, D. Gonzalez, R. Domingo, A. Pastor, D. Merodio, I. Conway. Adaptive Hardware and Systems (AHS), NASA/ESA Conference on, IEEE, pp. 1-8, Edinburgh, UK, August 2018

20 "*5G mm wave networks leveraging enhanced fiber-wireless convergence for high-density environments: the 5G-PHOS approach*.", Papaioannou, Kalfas, Vagionas, Maniotis, Miliou, Pleros, Neto, Chanclor, Raj-Ali, Bakopoulos, Caillaud, Debregeas, Sirbu, Eichhammer, Theodoropoulou, Lyberopoulos, Kartsakli, Vardakas, Torfs, Yin, Tsagkaris, Demestichas, Giannoulis, Avramopoulos, Lentaris, Varvarigos, Tafur Monroy, Dayan, Leiba, Dimogiannis, Kontogiannis, Magri, Tartaglia, Roeloffzen, Oldenbeuving, 2018 IEEE Int'l Symposium on Broadband Multimedia Systems and Broadcasting (BMSB). IEEE, Spain, June 2018

19 "*A Framework Exploiting Process Variability To Improve Energy Efficiency in FPGA Applications"*, K. Maragos, G. Lentaris, I. Stratakos, D. Soudris. ACM Great Lakes Symposium on VLSI (GLSVLSI), Proc. of, pp.87-92, Chicago, USA, May 2018

18 *"Carrier Phase Recovery of 64 GBd Optical 16-QAM Using Extensive Parallelization on an FPGA"*, Kostalampros, Maragos, Lentaris, Soudris, Spatharakis, Argyris, Avramopoulos, Dris. Circuits and Systems, IEEE I'ntl Symp. on (ISCAS), proc of., pp 1-5, Florence Italy, May 2018

17 *"Real-Time Carrier Phase Recovery for 16-QAM Utilizing the Nonlinear Least Squares Algorithm",* Kostalampros, Spatharakis, Maragos, Lentaris, Argyris, Dris, Richter, Avramopoulos, Soudris. Optical Fiber Communications Conference and Exhibition (OFC), IEEE, Proc. of., pp 1-3, California USA, March 2018

16 *"Project HIPNOS: Case Study of High Performance Avionics for Active Debris Removal in Space*", G. Lentaris, I. Stratakos, I. Stamoulias, K. Maragos, D. Soudris, M. Lourakis, X. Zabulis, D. Gonzalez-Arjona. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 350-355, Bochum Germany, July 2017

15 "*FPGA Acceleration of Hyperspectral Image Processing for High-Speed Detection Applications*", S. Vellas, G. Lentaris, K. Maragos, D. Soudris, Z. Kandylakis, K. Karantzalos. Circuits and Systems, IEEE I'ntl Symp. on (ISCAS), pp. 1-4, Baltimore USA, May 2017

14 "*Application Performance Improvement By Exploiting Process Variability On FPGA Devices*", K. Maragos, G. Lentaris, D. Soudris, K. Siozios, V. F. Pavlidis. Design, Automation & Test in Europe (DATE), IEEE Conf. on, pp. 452-457, Lausanne Switzerland, March 2017

13 "*SPARTAN/SEXTANT/COMPASS: Advancing Space Rover Vision via Reconfigurable Platforms*", Lentaris, Stamoulias, Diamantopoulos, Maragos, Siozios, Soudris, Aviles, Lourakis, Zabulis, Kostavelis, Nalpantidis, Boukas, Gasteratos, accepted, Applied Reconfigurable Computing (ARC) Symposium, Springer, Germany, April 2015.

12 "*Neuronal Connectivity Assessment for Epileptic Seizure Prevention: Parallelizing the*

Generalized Partial Directed Coherence on Many-Core Platforms", G. Georgis, D. Reisis, P. Skordilakis, K. Tsakalis, A. B. Shafique, G. Chatzikonstantis, G. Lentaris. Embedded Computer Systems (SAMOS), IEEE Int'l conf., Greece, 2014.

11 "*Low Complexity Interpolation Filters for Motion Estimation and Application to the H. 264 Encoders*", G. Georgis, G. Lentaris, D. Reisis. Design and Architectures for Digital Signal Processing (G. Ruiz, J. A. Michell), chapter 6, ISBN 978-953-51-0874-0, InTech, 2013

10 "*Single-Image Super-Resolution Using Low Complexity Adaptive Iterative Backprojection*", G. Georgis, G. Lentaris, D. Reisis. Digital Signal Processing, IEEE 18th Int'l conference on, Greece, July 2013.

9 "*FPGA-Based Path-Planning of High Mobility Rover for Future Planetary Missions*", G. Lentaris, D. Diamantopoulos, J. Stamoulias, K. Siozios, D. Soudris, M. A. Rodrigálvarez, Electronics Circuits and Systems, 19th IEEE Int'l Conf. on, pp. 192-195, Seville, Dec. 2012.

8 "*Hardware implementation of stereo correspondence algorithm for the Exomars mission*", G. Lentaris, D. Diamantopoulos, K. Siozios, D. Soudris, M. A. Rodrigálvarez, Field Programmable Logic and Applications (FPL), 22nd IEEE Int'l Conf. on, 29-31 August 2012.

7 "*SPARTAN project: On profiling computer vision algorithms for rover navigation*", D. Diamantopoulos, K. Siozios, G. Lentaris, D. Soudris, M. A. Rodrigalvarez, (2012, June). Adaptive Hardware and Systems (AHS), NASA/ESA Conf. on, IEEE, p. 174-181, June 2012

6 "*Configurable baseband digital transceiver for Gbps wireless 60 GHz communications*", D. Diamantopoulos, P. Galiatsatos, A. Karachalios, G. Lentaris, D. Reisis, D. Soudris. Electronics Circuits and Systems, 18th IEEE International Conf. on, pp. 192-195, Lebanon, Dec. 2011

5 "*Study of interpolation filters for motion estimation with application in H.264/AVC encoders",* G. Georgis, G. Lentaris, and D. Reisis. Electronics Circuits and Systems, 18th IEEE International Conference on, pp. 9-12, Beirut Lebanon, December 2011.

4 *"Customizing a VLIW Chip Multiprocessor for Motion Estimation Algorithms",* V. Chouliaras, G. Lentaris, D. Reisis, D. Stevens. Architecture of Computing Systems (ARCS'11), 24th Intl Conf on, PARMA Workshop, pp. 178-184, Italy, Feb 2011.

3 *"Programmable Motion Estimation architecture",* A. Drolapas, G. Lentaris, D. Reisis, IEEE Int'l Conference on Electronics, Circuits and Systems (ICECS 2009)

2 *"An Efficient H.264 VLSI Advanced Video Encoder"*, K. Babionitakis, G. Lentaris, K. Nakos, D. Reisis, N. Vlassopoulos, G. Doumenis, G. Georgakarakos, J. Sifnaios, IEEE International Conference on Electronics, Circuits and Systems (ICECS 2006)

C1 *"An approach for efficient design of digital amplifiers"*, N. Vlassopoulos. D. Reisis, G. Lentaris, G. Tombras. K. Tsakalis, N. Prosalentis, N. Ritas, International Symposium on Circuits and Systems (ISCAS 2006)

Publications (Submitted, In press)

5 *"Systematic Evaluation of the European NG-LARGE FPGA & EDA Tools for On-Board Processing",* V. Leon, I. Stamoulias, G. Lentaris, D. Soudris, R. Domingo, M. Verdugo, D. Gonzalez-Arjona, D. Merodio-Codinachs, I. Conway. European workshop on on-board data processing (OBDP2021), pp. 1-8, June 2021, in press (accepted)

4 "*Demonstration of FPGA-based A-IFoF/mmWave transceiver integration in mobile infrastructure for beyond 5G transport*", P. Toumasis, K. Kanta, K. Tokas, I. Stratakos, E. A. Papatheofanous, G. Giannoulis, I. Mesogiti, E. Theodoropoulou, G. Lyberopoulos, G. Lentaris, D. Apostolopoulos, D. Reisis, D. Soudris, H. Avramopoulos, IEEE conf. on Optical Communications (ECOC), Sept. 2021, submitted

3 "*Voltage Scaling and Guardband Customization of Multiple Constituent Components in SoC-FPGA*", Stratakos I, Maragos K, Lentaris G., in IEEE Int'l Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS) 2019, in press

2 Yuan, Fei, ed. Low Power Circuits for Emerging Applications in Communications, Computing, and Sensing. Book chapter 7, "*Aging evaluation and Mitigation Techniques Targeting FPGA devices*", I. Stratakos, K. Maragos, G. Lentaris, D. Soudris, K. Siozios. CRC Press, in press

S1 *"Design of a Real-Time DSP Engine on RF-SoC FPGA for 5G Networks",* V. Kitsakis, K. Kanta, I. Stratakos, G. Giannoulis, D. Apostolopoulos, G. Lentaris, H. Avramopoulos, D. Soudris, D. Reisis, Int'l Conf. on Optical Network Design & Modeling (ONDM 2019), in press

Talks/Presentations (Int'l conferences & workshops)

1. ACCEDE 2022: COTS components for space applications, ESA workshop, Seville Spain, hybrid/virtual presence, October 2022. *Talk*
2. IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Oct. 2022,

Patras, Greece. *Two talks (plus best paper award)*

3. European Network on High-performance Embedded Architecture and Compilation (HiPEAC), Workshop on Reconfigurable Computing (WRC), June 2022, Budapest, HU. *Invited Talk.*
4. IEEE International Symposium Circuits and Systems (ISCAS), May 2022, Texas, USA, Hybrid/virtual presence. *Poster presentation*
5. IEEE International Symposium on Circuits and Systems (ISCAS), May 2021, Korea, Virtual Conference. *Poster presentation*
6. European Network on High-performance Embedded Architecture and Compilation (HiPEAC), Workshop on Reconfigurable Computing (WRC), Virtual Conf., January 2021. *Invited Talk*
7. IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2020, Virtual Conference. *Poster presentation*
8. EASN: Innovation in Aviation & Space, 9th International conf. on, 2019, European Aeronautics Science Network (EASN), Athens, Greece. *Talk*.
9. ADCSS: Avionics, Data, Control and Software Systems, 12th workshop, 2018, European Space Research and Technology Center (ESTEC), ESA, The Netherlands. *Talk*.
10. Space-based LIDAR remote sensing techniques and emerging technologies, 2nd workshop, NASA/ESA/CNRS, Milos, Greece, 2018. *Poster presentation*.
11. SEFUW: SpacE FPGA Users 4th Workshop, 2018, European Space Research and Technology Center (ESTEC), ESA, The Netherlands. *Two Talks*.
12. Clean Space industrial days, Workshop, 2017, European Space Research and Technology Center (ESTEC), ESA, The Netherlands. *Talk*.
13. On-Line Testing (IOLTS), 23rd IEEE Int'l Symposium, 2017, Thessaloniki, Greece. *Talk*.
14. SEFUW: SpacE FPGA Users 3rd Workshop, 2016, European Space Research and Technology Center (ESTEC), ESA, The Netherlands. *Talk*.
15. SEFUW: SpacE FPGA Users 2nd Workshop, 2014, European Space Research and Technology Center (ESTEC), ESA, The Netherlands. *Talk and demonstration*.
16. Architecture of Computing Systems (ARCS) 2011, Italy. *Paper presentation*.
17. IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2009, Hammamet, Tunisia. *Presentation of three papers*.

Peer reviews (regular volunteer work)

IEEE Transactions on Circuits and Systems for Video Technology,
IEEE Transactions on Image Processing,
IEEE Transactions on Multi-Scale Computing Systems,
IEEE Transactions on Emerging Topics in Computing,
IEEE Transactions on Very Large Scale Integration Systems,
IET Image Processing,
Elsevier Microprocessors and Microsystems,
Elsevier Journal of The Franklin Institute,
AIAA Journal of Aerospace Information Systems,
World Scientific Journal of Circuits Systems and Computers,
EURASIP Journal on Wireless Communications and Networking,
IEEE Intl. Conf. On Electronics Circuits and Systems (ICECS),
IEEE Intl. Conf. On Computer Engineering and Systems (ICCES),
IEEE Intl. Symp. On Circuits and Systems (ISCAS).

Theses

* "*Parallel Architectures and Algorithms for Digital Signal and Image Processing*". Ph.D. Dissertation. Advisors: D. Reisis, A. Katsaggelos, G. Tombras, NKUA (2011).
* "*Models of Parallel Computation and Parallel Complexity*", MSc thesis supervised by asst. Prof. Dionysios Reisis, dpt. of Physics, NKUA, and Prof. Stathis Zachos, school of Electrical and Computer Engineering, NTUA (2010).
* "*Design and Implementation of algorithms for Motion Estimation and Motion Compensation*", MSc thesis supervised by asst. Prof. D. Reisis, dpt. of Physics, NKUA (2006).
* "*Computer architectures for Digital Signal Processing*", BSc thesis supervised by asst. Prof. Dionysios Reisis, dpt. of Physics, NKUA (2004)

Teaching experience

Assistant Professor (university)

- Signals and Systems course (ICE1-4006), dpt. of Informatics and Computer Engineering,

Univ. West Attica (2023)
- Advanced Computer Architecture course (ICE1-8202-Θ), dpt. of Informatics and Computer Engineering, Univ. West Attica (2023)

Teaching Associate (university)
- Academic Scholar on Digital Systems Design (adjunct professor on course ICE1-4005), dpt. of Informatics and Computer Engineering, Univ. West Attica (2021, 2022)
- Academic Scholar on Parallel Computation (adjunct professor on course ICE1-5006), dpt. of Informatics and Computer Engineering, Univ. West Attica (2020, 2021)
- Academic Scholar on Digital Circuit Design (adjunct professor on course ICE286, including research, paper C27), dpt. of Informatics & Computer Engineering, Univ. West Attica (2020)
- Lectures on Video Compression as part of the course Special Topics on Informatics of the graduate programme "Electronic Automation", Physics dpt., NKUA (2008-2021).
- Lectures on the course Digital Signal Processors, Informatics dpt., NKUA (2013-2014).
- Lectures on the course Embedded Systems, Informatics dpt., NKUA (2016).

Teaching Assistant (university)
- e-class lecture on FPGAs for space, EC H2020 project "Fabspace 2.0" (2018)
- lectures on FPGAs, DAAD project "TEACHER" and NTUA microlab courses (2016-2017)
- Lab assistant, under-graduate courses Computers I/II, Physics dpt., NKUA (2005-2008)

Mentoring (university)
- guidance of post- and under-graduate students on projects & theses, NKUA and NTUA.

Mentoring (student contests)
- guidance of student teams in Int'l contests (in *NASA SpaceApp* challenge, awarded-qualified Oct. 2019, as well as in *Intel InnovateFPGA* design contest, awarded-qualified Sept. 2019)

Research Interests

Parallel algorithms and architectures
Digital circuit design (FPGA, VLSI)
Space avionics and data handling
Embedded systems
Edge Computing
HW/SW co-design
Reliability of FPGA devices
Multi-/Many-core accelerators
Computer Architecture
Parallel memory organization
Theoretical informatics

with application in
Computer vision, Artificial Intelligence & Deep Learning (CNN, LSTM), Image processing, Video compression, Telecommunication, Active/passive sensing (LIDAR, cameras, etc.),Motion estimation, 1D and 2D interpolation and filtering, OFDM synchronization and baseband processing, FFT, Audio signal.