ADVANCED DESIGN AND SYNTHESIS OF DIGITAL SYSTEMS

1. GENERAL

SCHOOL	ENGINEERING		
SECTION	INFORMATICS & COMPUTER ENGINEERING		
LEVEL OF STUDIES	UNDERGRADUATE		
COURSE CODE		**SEMESTER OF STUDY**	8th
COURSE TITLE	ADVANCED DESIGN AND SYNTHESIS OF DIGITAL SYSTEMS		

INDEPENDENT TEACHING ACTIVITIES *in case the credits are awarded in distinct parts of the course e.g. Lectures, Laboratory Exercises, etc. If the credits are awarded uniformly for the entire course, indicate the weekly teaching hours and the total number of credits*	**WEEKLY HOURS TEACHING**	**CREDIT UNITS**
Lectures	3	
Laboratory	1	
Add rows if needed. The organization of teaching and the teaching methods used are described In detail at 4.	**4**	**5**

COURSE TYPE *Background, General Knowledge, Scientific Area, Development Skill*	Scientific Area, Skills Development
PREREQUISITES COURSES:	
LANGUAGE OF INSTRUCTION and EXAMINATION:	Greek
THE COURSE IS OFFERED TO ERASMUS STUDENTS	Yes
ONLINE COURSE PAGE (URL)	

2. LEARNING OUTCOMES

Learning Outcomes

The learning outcomes of the course are described, the *specific knowledge, skills and abilities* of *an appropriate level that students will acquire after the successful completion of the course.*

Consult Appendix A

- Description *of* the *Level* of *Learning Outcomes for each* course *of study according to the European Higher Education Area Qualifications Framework*
- *Descriptors of Levels 6, 7 & 8 of the European Qualifications Framework* for *Lifelong Learning and Annex B*
- *Summary Guide for writing Learning Outcomes*

Upon completion of the course, students will be able to

- They analyze digital circuits at both low and high frequencies.
- They design digital electronic circuits using FPGAs.
- Analyze and design digital systems and layouts implemented with FPGAs that interconnect with the real world through both analog and digital channels.

General Skills

Taking into account the *general competencies that* the *graduate must have acquired (as listed in* the *Diploma Supplement and listed below) which of them is the subject aimed at?*

Search, *analysis* and synthesis *of data and information, using the necessary technologies*	*Project planning and management*
Adapting to new situations Decision making	*Respect for diversity and multiculturalism Respect for the natural environment*
Autonomous work	*Demonstrate social, professional and ethical responsibility and sensitivity to gender issues Criticism and self-criticism*
Teamwork	*Promotion of free, creative and inductive thinking*

Working in an international environment
Working in an interdisciplinary environment

Generating new research ideas
• Autonomous Work • Promotion of creative and inductive thinking

3. COURSE CONTENT

The course is organized in four sections:

Module 1: FPGA-Based Systems, Digital Design and FPGAs, The Role of FPGAs, Types of FPGAs, FPGAs vs. Personalized VLSI Logic, Design in FPGA-Based Systems, Hierarchical Design, VLSI Technology , Processes Manufacturing, Characteristics of transistors, Logic gates, Static Supplementary Gates, Gate Delay, Design of Digital Systems in FPGA, Power Consumption, Driving High Loads, Low Power Gates, Interrupting Logic, Cables, Parasitic Cable Elements, Cable Models, Delay through an RC Transmission Line, Buffers Introduction) on the RC Transmission Line, Crosstalks Between RC Cables, Registers, Random Access Memories.

Module 2: FPGA Architectures, Permanently Programmed FPGAs , Antifuses, Flash Configuration, Logic Blocks, Interface Networks, Programming, Integrated I/O, FPGA Structure Circuit Design, FPGA Structure Architecture, Logic Parameters, Interface Architecture, Hardware Description Languages, Modeling with HDLs, Verilog , VHDL, Combined Network Delay, Delay Specifications, Gateway and Cable Delay, Trail Delay, Delay and Physical Design, Power & Energy Optimization, Malfunction Analysis and Optimization, Numerical Logic, Logic Implementation for FPGAs, Physical Planning for FPGAs, Review of the logical design process.

Module 3: Sequential Machines, Sequence Machine Design Process, State Transition and Plane Level Model – Register, Finite-State Machine Theory, State Assignment, Rules for Timing, Flip-Flop and Latches, Timing Principles, Performance Analysis, Performance of Flip-Flop-Based Systems , Performance of Systems based on Latches, Clock Skew, Retiming, Power Optimization, Combinatorial Logic Design, Data Path Controller Architecture, Scheduling and Distribution, Consumption, Pipeline, Design Methodologies.

Module 4: Very Large-Scale Systems, Channels, Protocols and Specifications, Logical Bus Design, Microprocessors and Bus Systems, FPGA Layout Architectures, Serial I/O, CPUs and Embedded Multipliers, Multi-FPGA Systems, Limitations of Multiple FPGAs, Multi-FPGAs Interface, Microprocessor and System Channels.

4. TEACHING AND LEARNING METHODS - ASSESSMENT

HOW TO DELIVER *Face-to-face, Remote education , etc.*	Face-to-face and remotely in terms of material for the creation and implementation of integrated circuits
USE OF INFORMATION TECHNOLOGIES AND COMMUNICATIONS *Use of ICT in Teaching, Laboratory Education, Communication with students*	• Posting of theoretical material (notes, lecture slides, exercises, topics examinations, etc.) on the e-learning platform (e-class). • Use of email and announcements on the e-learning platform for communication with students.

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<td>TEACHING ORGANIZATION
The way and methods of teaching are described in detail.
Lectures, Seminars, Laboratory Exercise, Field Exercise, Bibliography Study & Analysis, Tutorial, Practice (placement), Clinical Practicum, Art Workshop, Interactive teaching, Educational visits, Project preparation, Writing of work / assignments, Artistic creation, etc.

The student's study hours for each learning activity as well as the hours of unguided study are listed so that the total workload at semester level corresponds to ECTS standards</td>
<td>
<table>
<tr><th>Activity</th><th>Workload Semester</th></tr>
<tr><td>Lectures</td><td>39</td></tr>
<tr><td>Laboratory Exercises</td><td>13</td></tr>
<tr><td>Project</td><td>31</td></tr>
<tr><td>Independent Study</td><td>42</td></tr>
<tr><td>Course Total
(25 hours of load working per credit unit)</td><td>125</td></tr>
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<td>STUDENT EVALUATION
Description of the evaluation process

Assessment Language, Assessment Methods, Formative or Inferential, Multiple Choice Test, Short Answer Questions, Essay Development Questions, Problem Solving, Written Assignment, Report/Report, Oral Exam, Public Presentation, Laboratory Work, Clinical Patient Examination, Artistic Performance, Other / Other

Explicitly defined assessment criteria are indicated and if and where they are accessible to students.</td>
<td>I. Written final exam (70%) including :
- Short answer questions
- Multiple choice questions
- Solving exercises and problems

II. Elaboration of laboratory exercises and final laboratory examination (30%)

For successful completion, a grade of at least 5/10 is required both in the Written Final Exam and in the laboratory part of the course.

The syllabus to be examined and the evaluation process
They are communicated to students in the lecture hall, in the laboratory and in the e-class.</td>
</tr>
</table>

5. RECOMMENDED-BIBLIOGRAPHY

- Suggested Bibliography :

1. Wayne Wolf, Digital Systems Design in FPGAs, New Technologies Publications, 2013
2. Volnei A. Pedroni Hotels, Circuit Design with VHDL, Kleidarithmos Publications, 2008