Curriculum Vitae

Ioannis VOYIATZIS

PERSONAL DATA

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A. SCIENTIFIC DATA

A1. STUDIES

1. Ph.D. (1998). Department of Informatics, University of Athens; title of dissertation: “Built-in Self-Test Architectures for Digital Circuits in CMOS VLSI Technology”.
2. M.S. (1994). Department of Informatics, University of Athens.
3. B.S, Department of Informatics, University of Athens (1990).

A2. WORKS IN JOURNALS

J1. I. Voyiatzis, PASCHALIS A., NIKOLOS D., HALATSIS C., “An Efficient Built-In Self-Test Method for Robust Path Delay Fault Testing”, Journal of Electronic Testing: Theory and Applications, vol. 8, Issue 2, April 1996, pp. 219-222.

J2. I. Voyiatzis, PASCHALIS A., NIKOLOS D., HALATSIS C., “Accumulator-based BIST Approach for two-pattern testing”, Journal of Electronic Testing: Theory and Applications, Volume 15, Issue 3 (December 1999), pp. 267 - 278.

J3. I. Voyiatzis, “A Counter-Based Pseudo-Exhaustive Pattern Generator for BIST Applications”, the Microelectronics Journal, vol. 35, no 11, 2004, pp. 927-935.

J4. I. Voyiatzis, Paschalis A., Gizopoulos D., Kranitis N., Halatsis C., “A Concurrent BIST Scheme Based on a Self-Testing RAM”, IEEE Transactions on Reliability, Vol. 54, No. 1, March 2005, pp. 69-78.

J5. I. Voyiatzis, N. Kranitis, D. Gizopoulos, A. Paschalis, C. Halatsis, “An Accumulator-based Built-In Self-Test Generator for Robustly Detectable Sequential Fault Testing”, IEE Proceedings Computers & Digital Techniques, 2004, vol. 151, no. 6, pp. 466-472.

J6. I. Voyiatzis, HALATSIS C., “A low-cost Concurrent BIST scheme for increased Dependability”, IEEE Transactions on Dependable and Secure Computing, vol. 2, No 2, April 2005, pp. 150-156.

J7. I. Voyiatzis, GIZOPOULOS D., PASCHALIS A., “Accumulator-based test generation for robust sequential fault testing in DSP cores in near-optimal time”, IEEE Transactions on Very Large Scale Integration Systems, Sept. 2005, Vol. 13, Issue: 9, pp. 1079- 1086.

J8. I. Voyiatzis, “Test Vector Embedding into Accumulator-generated sequences: A Linear-Time Solution”, IEEE Transactions on Computers, vol. 54, no. 4, pp. 476–484, Apr. 2005.

J9. I. Voyiatzis, Th. Haniotakis, C. Halatsis, “A Novel Algorithm for the Generation of SIC Pairs and its Implementation in a BIST environment”, IEE Proc. Circuits, Devices & Systems, vol. 153, Issue 5, October 2006, pp. 427-432.

J10. I. Voyiatzis, D. Kehagias, “A SIC Pair Generator for a BILBO Environment”, Journal of Circuits, Systems and Computers, vol. 15, no. 5, October 2006, pp. 739-756.

J11. I. Voyiatzis, “Accumulator-based Pseudo-exhaustive two-pattern generation”, Journal of Systems Architecture, Elsevier publishers, vol. 53, Issue 11, pp. 846-860, Nov. 2007.

J12. I. Voyiatzis, “An ALU based BIST scheme for Word-organized RAMs”, IEEE Transactions on Computers, vol. 57, no. 8, August 2008, pp. 1012-1022.

J13. I. Voyiatzis, “On Embedding Test patterns into Low-Power BIST sequences”, Journal of Computer Information Systems, vol. XLIX, no. 2, Winter 2008-2009, pp. 58-64.

J14. I. Voyiatzis, "An Accumulator - based compaction scheme with reduced aliasing for on-line BIST of RAMs", IEEE Transactions on VLSI Systems, vo. 16, no. 9, September 2008, pp. 1248-1251.

J15. I. Voyiatzis, “A Low-cost BIST Scheme for Test Vector Embedding in Accumulator-Generated Sequences”, VLSI Design, Volume 2008, Issue 2 (January 2008) Article No. 4.

J16. I. Voyiatzis, A. Paschalis, D. Gizopoulos, C. Halatsis, E. Makri, M. Hatzimihail, “An Input Vector Monitoring Concurrent BIST Architecture Based on a Pre-computed Test Set”, IEEE Transactions on Computers, Volume 57, Issue 8, Aug. 2008, pp.1012 - 1022.

J17. I. Voyiatzis, D. Gizopoulos, A. Paschalis, “Recursive Pseudo-Exhaustive Two-pattern Generation”, IEEE Transactions on VLSI Systems, vol. 18, Issue 1, Jan. 2010, pp. 142-152.

J18. I. Voyiatzis, C. Efstathiou, “An Efficient Architecture for Accumulator-Based Test Generation of SIC pairs”, Volume 41 Issue 8, August, 2010, Elsevier Science Publishers.

J19. D. Magos, I. Voyiatzis, S. Tarnick, “An Accumulator-Based Test-per-clock Scheme”, IEEE Transactions on VLSI Systems, June 2011, Volume: 19, Issue: 6, pp: 1090 – 1094.

J20. A. Paschalis, I. Voyiatzis, D. Gizopoulos, «Accumulator based 3-Weight Pattern Generation», IEEE Transactions on VLSI Systems, Volume: 20, Issue: 2, pp. 357 – 361.

J21. I. Voyiatzis, H. Antonopoulou, C. Efstathiou, “A Low-Cost Optimal Time Sic Pair Generator”, Radioelectronics & Informatics, № 4 (51), September – December 2010.

J22. I. Voyiatzis, C. Efstathiou, H. Antonopoulou, A. Milidonis, “An Arithmetic Module-Based BIST Architecture for Two-Pattern Testing”, accepted for publication in IET Computers & Digital Techniques.

J23. I. Voyiatzis, C. Efstathiou, H. Antonopoulou, A. Milidonis, "An Effective Two-Pattern Test Generator For Arithmetic BIST", Computers and Electrical Engineering, Elsevier Publishers, Volume 39, Issue 2, February 2013, Pages 398–409.

J24. C. Efstathiou, N. Moschopoulos, I. Voyiatzis, K. Pekmestzi, "On the Design Of Modulo 2n + 1 Dot Product And Generalized Multiply-Add Units", Computers And Electrical Engineering, Elsevier Publishers, Volume 39, Issue 2, February 2013, Pages 410–419.

J25. I. Voyiatzis, C. Efstathiou, "Input Vector Monitoring Concurrent BIST architecture using SRAM Cells", Very Large-Scale Integration (VLSI) Systems, IEEE Transactions on (Volume: 22, Issue: 7), Page(s): 1625 – 1629.

J26. I. Voyiatzis, “Aliasing Reduction in Accumulator-based Response Verification”, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on (Volume: 33, Issue: 11), Page(s): 1746 – 1750.

J27. I. Voyiatzis, D. Kavvadias, “On the Generation of SIC Pairs in Optimal Time”, Computers, IEEE Transactions on (Volume: 64, Issue: 10), Page(s): 2891 – 2901, Oct. 2015.

J28. Troussas, C., Giannakas, F., Sgouropoulou, C., Voyiatzis, I., Collaborative activities recommendation based on students’ collaborative learning styles using ANN and WSM, Interactive Learning Environments, 2020.

J29. Nikolopoulos, D., Petraki, E., Yannakopoulos, P.H., (...), Voyiatzis, I., Cantzos, D., Long-lasting patterns in 3 KHZ electromagnetic time series after the Ml = 6.6 earthquake of 2018-10-25 near zakynthos, Greece, Geosciences (Switzerland), 10(6),235, pp. 1-24, 2020.

J30. D’Incecco, S.; Di Carlo, P.; Aruffo, E.; Chatzisavvas, N.; Petraki, E.; Priniotakis, G.; Voyiatzis, I.; Yannakopoulos, P.H.; Nikolopoulos, D. Fractal Dimension Analysis Applied to Soil CO2 Fluxes in Campotosto’s Seismic Area, Central Italy. Geosciences 2020, 10, 233. https://doi.org/10.3390/geosciences10060233.

J31. Troussas, C., Krouska, A., Sgouropoulou, C., Voyiatzis, I., Ensemble learning using fuzzy weights to improve learning style identification for adapted instructional routines, Entropy, 22(7),735, 2020.

J32. Giannakas, F., Troussas, C., Voyiatzis, I., Sgouropoulou, C., “A deep learning classification framework for early prediction of team-based academic performance”, Applied Soft Computing, 106,107355, 2021.

A3. PUBLICATIONS IN INTERNATIONAL CONFERENCES

C1. I. Voyiatzis, Nikolos D., Paschalis A., Halatsis C., Haniotakis Th., "An Efficient Comparative Concurrent Built-In Self-Test Technique", 4th IEEE Asian Test Symposium in Bangalore, India, 1995.

C2. I. Voyiatzis, Paschalis A., Nikolos D., Halatsis C., "Accumulator-Based BIST Approach for Stuck-Open and Delay Fault Testing", European Test Conference, pp. 431-435, Paris, France, March 6-9, 1995.

C3. I. Voyiatzis, Paschalis A., Nikolos D., Halatsis C., "R-CBIST: An Efficient Concurrent BIST Technique", IEEE International Test Conference, 1998.

C4. I. Voyiatzis, Paschalis A., Nikolos D., Halatsis C., "Exhaustive and Pseudoexhaustive Built-In Two-Pattern Generation for Datapaths", Proc. of the 4th IEEE On-Line Testing Workshop, pages 90-94, 1998.

C5. I. Voyiatzis, Kranitis N., Paschalis A., Gizopoulos D., Halatsis C., "ALU-based Built-In Self-Test Generator for Transition Fault Testing", IEEE European Test Workshop, 2002.

C6. I. Voyiatzis, Gizopoulos D., Paschalis A., "Accumulator-based Weighted Pattern Generation", in IEEE International On-Line test Symposium, July 2005.

C7. I. Voyiatzis, Gizopoulos D., Paschalis A., Halatsis C., "A Concurrent BIST scheme for online/offline testing based on a precomputed test set", IEEE International Test Conference, November 2005.

C8. I. Voyiatzis, "Accumulator-based compression in Symmetric Transparent RAM BIST", in IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Technology, 2006.

C9. I. Voyiatzis, "On Embedding Test patterns into Low-Power BIST sequences", in IEEE International On-Line Test Symposium 2007, pp. 197-198.

C10. I. Voyiatzis, Antonopoulou H., "Decoder-based Decompression for test sets containing don't cares", in IEEE Conference on Design and Technology of Integrated Systems in Deep Submicron Technology (DTIS 07).

C11. I. Voyiatzis, Kavvadias D., Antonopoulou H., Sinitos S., "Reliability considerations in Mobile Devices", Third ACM International Mobile Multimedia Communications Conference, article no. 51, 2007.

C12. I. Voyiatzis, Efstathiou C., «Two-pattern generation based on Accumulators with 1's Complement adders", in IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Technology, 2006.

C13. I. Voyiatzis, C. Efstathiou, "An Efficient Architecture for Accumulator-Based Test Generation of SIC pairs", in IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Technology, 2008.

C14. I. Voyiatzis, "On Reducing Aliasing in Accumulator-Based Compaction" in IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Technology, 2008.

C15. D. Magos, I. Voyiatzis, S. Tarnick, "A Low-cost Accumulator-based Test-pattern generation Architecture", IEEE International On-Line Test Symposium, 2008.

C16. I. Voyiatzis, D. Gizopoulos, A. Paschalis, "A Concurrent BIST scheme exploiting don't care values", in the 16th IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SOC), 2008.

C17. I. Voyiatzis, H. Antonopoulou, C. Efstathiou, "A Low-Cost Optimal Time SIC Pair Generator", 6th IEEE East-West Design and Test Symposium (EWDTS), 2008.

C18. C. Efstathiou, I. Voyiatzis, N. Sklavos, "On the modulo 2^n+1 multiplication for diminished-1 operands", 2nd International Conference on Signals, Circuits & Systems (SCS), 2008.

C19. I. Voyiatzis, Antonopoulou H., Efstathiou C., «Output Response Compaction in RAS-based Schemes", IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Technology, 2009.

C20. I. Voyiatzis, Gizopoulos D., Paschalis A., "An Input Vector Monitoring Concurrent BIST scheme Exploiting "X" values", in the IEEE International On-Line Test Symposium, 2009.

C21. C. Efstathiou, I. Voyiatzis, Prentakis M., "Design methods for modulo 2n+1 multiply-add units", 7th IEEE East-West Design and Test Symposium (EWDTS), 2009.

C22. N. Ioannidis, I. Voyiatzis, "Embedding Test patterns in Accumulator-Generated sequences in O(1) time", 13th Panhellenic Conference on Informatics, IEEE Proceedings, Corfu, Greece, 2009, pp. 55-59.

C23. C. Efstathiou, I. Voyiatzis, "Handling zero in diminished-1 modulo 2n + 1 subtraction", 3rd International Conference on Signals, Circuits & Systems (SCS), 2009.

C24. I. Voyiatzis, Th. Haniotakis, C. Efstathiou, H. Antonopoulou, "A Concurrent BIST architecture based on Monitoring Square Windows", IEEE Conference on Design & Techology in Nanoscale Era, 2010.

C25. D. Kavvadias, S. Sinitos, I. Voyiatzis, H. Antonopoulou, C. Efstathiou, “On Embedding Test Sets into Hardware Generated Sequences”, Panhellenic Conference on Informatics (PCI), IEEE Proceedings, Tripolis, Greece, September 2010.

C26. C. Efstathiou, I. Voyiatzis, “On the modulo 2n+1 subtract units for weighted operands”, International Conference on Microelectronics (ICM), 19-22 December 2010, Cairo, Egypt.

C27. C. Efstathiou, I. Voyiatzis, «On the diminished-1 modulo 2n+1 fused multiply-add units», in the 6th Conference on Design and Technology of Integrated Systems in nanoscale era, DTIS 2011.

C28. I. Voyiatzis, C. Efstathiou, H. Antonopoulou, G. Saousopoulos, K. Galanou,” Low-Overhead Two-dimensional test pattern generation", 6th Conference on Design and Technology of Integrated Systems in nanoscale era, DTIS 2011.

C29. I. Voyiatzis, C. Efstathiou, H. Antonopoulou, «A Novel SRAM-Cell based Input Vector Monitoring Concurrent BIST architecture», IEEE European Test Symposium, Trondheim, Norway, May 22-28, 2011.

C30. I. Voyiatzis, “Input Vector Monitoring on Line Concurrent BIST based on multilevel decoding logic”, in Design, Automation and Test in Europe Conference, 2012, Dresden, Germany.

C31. I. Voyiatzis, C. Efstathiou, K. Sgouropoulou, S. Hamdioui, «ALU Based Address Generation for RAMs», in the 7th IEEE Conference on Design and Technology of Integrated Systems in nanoscale era, DTIS 2012.

C32. I. Voyiatzis, C. Efstathiou, Y. Tsiatouhas, K. Sgouropoulou, “A Novel Architecture to Reduce test time in March-based SRAM tests”, in the 7th IEEE Conference on Design and Technology of Integrated Systems in nanoscale era, DTIS 2012.

C33. I. Voyiatzis, C. Efstathiou, K. Sgouropoulou, “Test vector Embedding in Accumulators with Stored Carry in O(1) time”, in the 7th IEEE Conference on Design and Technology of Integrated Systems in nanoscale era, DTIS 2012.

C34. I. Voyiatzis, D. Magos, C. Efstathiou, K. Sgouropoulou, “Test Set Embedding into Low-power sequences based on a Traveling Salesman problem formulation”, in the 7th IEEE Conference on Design and Technology of Integrated Systems in nanoscale era, DTIS 2012.

C35. I. Voyiatzis, K. Axiotis, N. Papaspyrou, H. Antonopoulou, C. Efstathiou, “Test Set Embedding Into Low-power BIST Sequences using Maximum Bipartite Matching”, in the 16th Panhellenic Conference on Informatics, PCI 2012.

C36. I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Symmetric Transparent Online BIST for Arrays of Word-Organized RAMs", ιn τhe 8th IEEE Conference on Design and Technology Of Integrated Systems In Nanoscale Era, DTIS 2013.

C37. I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Embedding Test Vectors In Accumulator - Based TPG Using Progressive Search", in the 8th IEEE Conference On Design And Technology Of Integrated Systems In Nanoscale Era, DTIS 2013.

C38. I. Voyiatzis, C. Efstathiou, C. Sgouropoulou and D. Magos, "Input vector monitoring concurrent BIST with Low hardware overhead", in the Second Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale (MEDIAN'13) Avignon, France, May, 2013, in conjunction with European Test Symposium.

C39. I. Voyiatzis, C. Efstathiou and C. Sgouropoulou, " A low-cost input vector monitoring concurrent BIST Scheme" in the IEEE On-line Test Symposium, Chania, Greece, July 2013.

C40. I. Voyiatzis, C. Sgouropoulou, C. Efstathiou, S. Neophytou, M. Michael, S. Hadjitheophanous, "Test set Embedding into Accumulator-generated sequences Targeting Hard-to-detect faults", IEEE International Design and Test Symposium, Marrakech, Morroco, December 2013.

C41. I. Voyiatzis, C. Sgouropoulou, C. Efstathiou, "Transparent Testing for Intra-Word Memory faults", IEEE International Design and Test Symposium, Marrakech, Morroco, December 2013.

C42. I. Voyiatzis, "Accumulator-based Test-per-clock Scheme for Low-power On-chip Application of Test patterns", 2014 IEEE European Test Symposium, May 26-30, 2014, Paderborn, Germany.

C43. I. Voyiatzis, "Concurrent Online BIST for Sequential circuits Exploiting Input Reduction and output Space Compaction", 2014 IEEE European Test Symposium, May 26-30, 2014, Paderborn, Germany.

C44. I. Voyiatzis, Costas Efstathiou, Cleo Sgouropoulou, "Accumulator-based Self-adjusting Output Data Compression for embedded Word-Organized DRAMs", 9th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS 2014), May 6-8, Santorini, Greece.

C45. I. Voyiatzis, Costas Efstathiou, Cleo Sgouropoulou, "Low overhead Output Response Compaction in RAS Architectures", 9th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS 2014), May 6-8, Santorini, Greece.

C46. C. Efstathiou, K. Tsoumanis, K. Pekmestzi, I. Voyiatzis, «On the Design of Efficient Modulo 2^n+1 Multiply-Add-Add Units», 9th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS 2014), May 6-8, Santorini, Greece.

C47. I. Nikopoulos, A. Milidonis, C. Efstathiou, C. Sgouropoulou, I. Voyiatzis, “Stealth Assessment of Hardware Trojans in simple Processors” in the ACM proceedings of PCI, October 2014, Athens, Greece.

C48. I. Voyiatzis, C. Sgouropoulou, C. Efstathiou, A Concurrent BIST Scheme for Read Only Memories, 10th Conference Design and Technology in deep nanoscale era (DTIS 2015).

C49. I. Voyiatzis, C. Sgouropoulou, C. Efstathiou, Detecting Untestable Hardware Trojan with Non-intrusive Concurrent On-Line testing, 10th Conference Design and Technology in deep nanoscale era (DTIS 2015).

C50. I. Voyiatzis, D. Kavvadias, S. Sinitos, K. Vlahantonis, Cleo Sgouropoulou, C. Efstathiou, “Test set Embedding into Hardware generated sequences using an Embedding Algorithm”, 10th Conference Design and Technology in deep nanoscale era (DTIS 2015).

C51. I. Voyiatzis, Symmetric Transparent On-Line BIST of word-organized memories with Binary Adders, 20th IEEE European Test Symposium, (ETS 2015).

C52. I. Voyiatzis and C. Efstathiou, “Accumulator-based Generation for Serial TPG”, 19th Panhellenic Conference on Informatics (PCI 2015).

C53. I. Voyiatzis and C. Efstathiou, “On the use of hard faults to generate test sets”, 19th Panhellenic Conference on Informatics (PCI 2015).

C54. I. Voyiatzis, C Efstathiou, “Low Cost Boolean Function generation”, 20th Panhellenic Conference on Informatics (PCI2016).

C55. I. Voyiatzis, C. Efstathiou, K. Patriarcheas, «Software-based SIC pair Generation», 20th Panhellenic Conference on Informatics (PCI2016).

C56. Voyiatzis, I., Efstathiou, C., On the generation of binary functions with low-overhead, Proceedings - 2017 12th IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2017, 7930167.

C57. Voyiatzis, I., Sgouropoulou, C., Airo Farulla, G., Processor-based Symmetric Transparent BIST, Proceedings - 2017 12th IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era, DTIS 2017, 7930173.

C58. Sgouropoulou, C., Voyiatzis, I., Koutoumanos, A., (...), Delgado Kloos, C., Garcia, R.C., Standards-based tools and services for building lifelong learning pathways, IEEE Global Engineering Education Conference, EDUCON, 7943065, pp. 1619-1621, 2017.

C59. Voyiatzis, I., SIC pair generation in optimal time using rotatable counters, Proceedings of the European Test Workshop, 7968240, 2017.

C60. Voyiatzis, I., Efstathiou, C., SIC pair generation in near-optimal time with carry-look ahead adders, Proceedings - 2018 13th IEEE International Conference on Design and Technology of Integrated Systems In Nanoscale Era, DTIS 2018.

C61. Voyiatzis, I., Efstathiou, C., Sgouropoulou, C., Programmable logic for single-output functions, Proceedings - 2018 13th IEEE International Conference on Design and Technology of Integrated Systems In Nanoscale Era, DTIS 2018.

C62. Galliakis, M., Skourlas, C., Galiotou, E., Voyiatzis, I., A low-cost smart home for the assistance of elderly persons and patients, ACM International Conference Proceeding Series, pp. 93-98, 2018

C63. Mourgelas, C., Kokkinos, S., Milidonis, A., Voyiatzis, I., Autonomous drone charging stations: A survey, ACM International Conference Proceeding Series, 2020

C64. Psilias, D., Milidonis, A., Voyiatzis, I., Architecture for Secure UAV Systems, ACM International Conference Proceeding Series, 2020

C65. Voutsinas, S., Karolidis, D., Voyiatzis, I., Samarakou, M., Development of an IoT seismograph, ACM International Conference Proceeding Series, 2020

C66. Troussas, C., Krouska, A., Giannakas, F., Sgouropoulou, C., Voyiatzis, I., Redesigning teaching strategies through an information filtering system, ACM International Conference Proceeding Series, 2020

C67. Troussas, C., Krouska, A., Giannakas, F., Sgouropoulou, C., Voyiatzis, I., Automated reasoning of learners' cognitive states using classification analysis, ACM International Conference Proceeding Series, 2020

C68. Voutsinas, S., Karolidis, D., Voyiatzis, I., Samarakou, M., A survey of fault detection and identification methods for Photovoltaic systems based on I-V curves, ACM International Conference Proceeding Series, 2020, T. Michailidis, E., G. Kogias, D., Voyiatzis, I.,

C69. A Review on Hardware Security Countermeasures for IoT: Emerging Mechanisms and Machine Learning Solutions, ACM International Conference Proceeding Series, 2020.

C70. Troussas, C., Krouska, A., Giannakas, F., Sgouropoulou, C., Voyiatzis, I., Representation of Generalized Human Cognitive Abilities in a Sophisticated Student Leaderboard, Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 12677 LNCS, pp. 398-405, 2021.

C71. Giannakas, F., Troussas, C., Krouska, A., Sgouropoulou, C., Voyiatzis, I., XGBoost and Deep Neural Network Comparison: The Case of Teams' Performance, Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics), 12677 LNCS, pp. 343-349, 2021.

C72. Voutsinas, S., Karolidis, D., Voyiatzis, I., Samarakou, M., Photovoltaic Faults: A comparative overview of detection and identification methods, 2021 10th International Conference on Modern Circuits and Systems Technologies, MOCAST 2021.

C73. Krouska, A., Troussas, C., Giannakas, F., Sgouropoulou, C., Voyiatzis, I., Enhancing the effectiveness of intelligent tutoring systems using adaptation and cognitive diagnosis modeling, Frontiers in Artificial Intelligence and Applications, 338,40-45, pp. V-VI, 2021.

C74. Troussas, C., Krouska, A., Giannakas, F., Sgouropoulou, C., Voyiatzis, I., An alternative educational tool through interactive software over facebook in the era of COVID-19, Frontiers in Artificial Intelligence and Applications, 338,3-10, pp. V-VI, 2021.

C75. S. Voutsinas, D. Karolidis, I. Voyiatzis, M. Samarakou, Development of a fault detection algorithm for Photovoltaic Systems, ACM International Conference Proceeding Series, PCI 2021

C76. S. Voutsinas, D. Karolidis, I. Voyiatzis, M. Samarakou, Development of an IoT Structural Damage Monitoring system, ACM International Conference Proceeding Series, PCI 2021

C77. I. Galanakis, A. Milidonis, I. Voyiatzis, A high-performance architecture for object detection in drones, ACM International Conference Proceeding Series, PCI 2021

C78. D. Psilias, A. Milidonis and I. Voyiatzis, Secure Video Transmission System for UAV Applications, ACM International Conference Proceeding Series, PCI 2021

C79. E. Gkini, I. Voyiatzis and C. Sgouropoulou, Head-Mounted Display Systems as Visual Aids for the Visually Impaired: A Survey, ACM International Conference Proceeding Series, PCI 2021

C80. A. Chalkiadaki, C. Mourgelas, D. Psilias, A. Milidonis, I. Voyiatzis, A survey for UAV open-source telemetry protocols, ACM International Conference Proceeding Series, PCI 2021

A4. PARTICIPATION IN EUROPEAN AND NATIONAL PROJECTS

- 1991-1993: ESPRIT 5692, Hellenic VLSI Design and Prototyping Environment.
- 1993-1995: STRIDE 187 "Hellenic Environment for Design and Manufacturing Prototype VLSI circuits".
- 2006-2008: European Community and Greek Government Project EPEAEK: "Support of Computer Science Studies in the Technological Educational Institution of Athens".
- 2005-2006: European Community and Greek Government Project Archimedes: "VLSI design and testing of functional modules for Digital Signal Processors and cryptography systems based on residue number arithmetic".
- 2005-2007: European Community and Greek Government Long-Life Learning Project EQUAL, Incorporation of mechanisms and programs of lifelong learning in Small and Medium Enterprises – Certification of educational material in the fields of Informatics and Technical professions Ekp@deyteite".
- 2012-2014: Archimedes, "Photonic Networks based on Photonic Integrated Circuits", European Community and Greek Government Project, Grant: 83.000€.
- 2012-2014: Archimedes, "Design and implementation of efficient Arithmetic units for non-conventional Number systems", European Community and Greek Government Project, Grant: 83.000€.
- 2014-2015: "ECVET-STEP: ECVET for Strengthening Training to Employment Pathways" συγχρηματοδοτούμενο από το Ευρωπαϊκό πρόγραμμα LLP Development of Innovation και το ΤΕΙ Αθήνας, Project No. 539815-LLP-1-2013-1-GR-LEONARDO-LMP.
- 2014-2015: "ACT: Agricultural Alliance for Competence and Skills based Training" LLP Development of Innovation, Project No. 540426-LLP-1-2013-1-DE-LEONARDO-LMP.
- 2014-2017: "DIGI-FEM: Digital Skills and Tools for Young Female Entrepreneurs" χρηματοδοτούμενο από το Ευρωπαϊκό πρόγραμμα Erasmus+, Project No. 2014-1-EL01-KA202-001401.
- 2015-2018: "Composing Lifelong Learning Opportunity Pathways through Standards-based Services (COMPASS)" χρηματοδοτούμενο από το Ευρωπαϊκό πρόγραμμα Erasmus+, Project No. 2015-1-2015-1-EL01-KA203-014033.
- 2017-2020: Sector Skills Alliance for the design and delivery of innovative VET programmes to Data Science and Internet of Things professionals (SEnDIng), Erasmus+ KA2: Cooperation for innovation and the exchange of good practices - Sector Skills Alliances, EU grant: 982.537 €
- 2018-2022: SmartPV, ΕΡΕΥΝΩ – ΔΗΜΙΟΥΡΓΩ – ΚΑΙΝΟΤΟΜΩ, συγχρηματοδοτείται από την Ευρωπαϊκή Ένωση και εθνικούς πόρους μέσω του Ε.Π. Ανταγωνιστικότητα, Επιχειρηματικότητα & Καινοτομία (ΕΠΑνΕΚ) (κωδικός έργου: Τ1ΕΔΚ-01485), total grant: 972.382,41 €.
- 2019-2022: Biocomp, Investigation and acquisition of necessary skills in bio-based economy, Erasmus+ KA2: Cooperation for innovation and the exchange of good practices, KA202 - Strategic Partnerships for vocational education and training, EU grant: 298.245,00 €.
- 2019-2022: SUMHEIS Project – Summer School Development Programme for European HEIs" project, financed under ERASMUS+ Programme, Key Action 2 – KA203 – Strategic Partnerships for higher education (project reference number 2019-1-IT02-KA203-062984), EU grant: 298.245,00€

A5. REVIEWER IN SCIENTIFIC JOURNALS AND CONFERENCES

- IEEE Transactions on Computers
- IEEE Transactions on Computer-Aided Design of Circuits and Systems
- IEE Proceedings: Computers and Digital Techniques
- IEEE European Design & Test Conference

- IEEE VLSI Test Symposium
- Journal of Electronic Testing: Theory and Applications
- Computers and Electrical Engineering
- Panhellenic Conference on Informatics
- International Conference on Signals, Circuits and Systems (SCS), Technically Sponsored by IEEE, Circuits and Systems Society
- International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), Technically sponsored by IEEE Circuits and Systems Society

A6. Conference Committee Member

A6.1 Program Committee Member:

- International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), Technically sponsored by IEEE Circuits and Systems Society 2007-2012.
- International Conference on Signals, Circuits and Systems (SCS), Technically Sponsored by IEEE, Circuits and Systems Society
- IEEE International On-line Test Symposium

A6.2 Steering Committee Member:

- International Conference on Design and Technology of Integrated Systems in Nanoscale Era 2011, Technically sponsored by IEEE Circuits and Systems Society, 2008-
- Panhellenic Conference on Informatics (PCI) 2008-

A6.3 Technical Chair:

- International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS) Technically sponsored by IEEE Circuits and Systems Society, 2010

A6.4 General Chair:

- International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS) Technically sponsored by IEEE Circuits and Systems Society, 2011.
- International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS) Technically sponsored by IEEE Circuits and Systems Society, 2014.

B. Working Experience

B1. Current Position

University of West Attica, Professor, Department of Informatics and Computer Engineering

B.2 Teaching Experience

- 1998-1999: University of Athens, Department of Informatics and Telecommunications.
- 2004-2005: University of Athens, Department of Mathematics, Visiting Professor
- 2005-2018: Technological Educational Institute of Athens, Department of Informatics
- 2014-2018: Department of Informatics and Telematics, Harokopian University of Athens
- 2018-: University of West Attica, Department of Informatics and Computer Engineering

C. Other Info

C1. Foreign Languages

ENGLISH (CERTIFICATE OF PROFICIENCY IN ENGLISH, UNIVERSITY OF CAMBRIDGE)

FRENCH (CERTIFICAT DE LANGUE FRANCAISE).

C3. MEMBERSHIP IN ASSOCIATIONS

2000 - : Greek Computer Society, Member

2004 - : Greek Computer Society, Member of the Board

2008 - 2011: Greek Computer Society, General Secretary of the Board

2011 - : Greek Computer Society, President of the Board

2005 - : Member, IEEE

2009 - : Member, ACM

2008 - : Member, TTTC of IEEE